## REMARKS

Claims 1-22, 24-26 and 28-34 are pending in this application. Claims 1-19 are withdrawn from consideration. By this Amendment, claims 23 and 27 are cancelled and claims 20-22, 24-26 and 28-34 are amended. Attached hereto is a marked-up version of the changes to the claims by the current amendment. The attachment is captioned **"Version with markings to show changes made."** Various amendments have been made to the claims, and for reasons unrelated to patentability. Unless specifically addressed below, each of these amendments is to provide further clarity and/or to refocus specifically claimed features.

Entry of this Amendment is proper under 37 C.F.R. §1.116 because the Amendment: a) places the application in condition for allowance for the reasons set forth below; b) does not raise any new issues requiring further search and/or consideration; and c) places the application in better form for an Appeal should an Appeal be necessary. More specifically, independent claims 20, 22, 26 and 29 are amended to include features previously recited in dependent claim 23. Independent claim 20 is also amended to recite features previously recited in dependent claim 25. Additionally, independent claim 22 is amended to more positively recite previously recited features. Finally, independent claims 26 and 29 are amended to add features previously recited in claim 22. Thus, all the amended features are believed to have been previously considered and do not raise any new issues requiring further search and/or consideration. Entry is proper under 37 C.F.R. §1.116.

The Office Action objects to claim 27 as being of improper dependent form. By this Amendment, dependent claim 27 is deleted. Thus, the objection is moot.

The Office Action rejects claim 34 under 35 U.S.C. §112, second paragraph. By this Amendment, "a third metal layer" is amended to "a first ruthenium film" and "a

fourth metal layer" is amended to "a second ruthenium film". Support for the claim 34 amendment is provided at least in paragraph [0080] of the Substitute Specification. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph, is respectfully requested.

The Office Action rejects claim 20, 21 and 26-28 under 35 U.S.C. §103(a) over U.S. Patent 5,837,578 to Fan et al. (hereafter Fan) in view of U.S. Patent 6,316,802 to Schindler et al. (hereafter Schindler). The Office Action also rejects claims 22-25 and 29-33 under 35 U.S.C. §103(a) over Fan in view of U.S. Patent 5,854,104 to Onishi et al. (hereafter Onishi). The rejections are respectfully traversed.

The present inventors have determined that the reliability between an upper electrode and a plug is improved by forming the upper electrode including a ruthenium film 47 and an oxidation resistance metal film 48 on the ruthenium film 47, and forming the oxidation resistance metal film 48 by a spattering method. For example, as discussed in the Substitute Specification at paragraph [0095] and as shown in Fig. 16, the ruthenium film 47 does not suck oxygen from the ashing atmosphere. Furthermore, since the tungsten film 48 has sufficient oxidation resistance and since suction of oxygen does not occur, the material that invites connection defects, such as titanium oxide, is not formed between the plug and the upper electrode 49. Additionally, as discussed in paragraph [0082] and shown in Fig. 9, when the CVD process is employed to deposit the tungsten film 48, the CVD atmosphere contains hydrogen and therefore becomes reducing. There is the possibility that hydrogen permeates through the ruthenium film 47 and reaches a BST film 46. Consequently, the tungsten film 48 is formed by sputtering.

Still further discussed at [0077] and shown in Fig. 8, when the CVD process is

used to deposit the ruthenium film 47, the spaces between the lower electrodes 45 processed very delicately can be buried in an excellent way. Additionally, the film thickness T2 of the tungsten film 48 may be greater than the film thickness T1 of the ruthenium film 47. When T2>T1, the overall stress of the upper electrode 49 can be reduced and the resistance of the upper electrode 49 can be further reduced. See paragraphs [0083]-[0084] and Fig. 9.

Independent claim 20 recites depositing a dielectric capacitance insulating film to cover the first electrodes, and depositing further a ruthenium film and a conductor layer by a spattering method. Claim 20 further recites patterning the ruthenium film and conductor layers to form second electrodes, and depositing a third inter-layer insulating film covering the second electrodes, and forming a first connection hole reaching the second electrode and a second connection hole reaching the first layer wiring by etching and wherein the conductor layer comprises a tungsten film and the third inter-layer insulating film comprises a silicon oxide film.

The applied references do not teach or suggest all the features of independent claim 20, or the similarly recited features in each of independent claims 22, 26 and 29.The Office Action relies of Fan as a primary reference and then relies on either Schindler or Onishi for missing features of Fan. However, as will be described below, the applied references do not teach or suggest all the features of the pending claims.

Fan describes forming a capacitor having a second conductive layer 391 as a lower electrode, a dielectric film 310 and a third conductive film 311 as an upper electrode. See Fan's col. 6, lines 26-65; and Figs. 3(h) - (j). The upper electrode 311 is formed in plural trenches. Fan does not teach or suggest forming upper electrode (311) buildup conductive layers. Additionally, Fan does not teach or

suggest a ruthenium film as the upper electrode.

Schindler describes forming an upper electrode of a capacitor having a platinum layer 23a as a first metal film and a tungsten layer 23b as a second metal film. The tungsten layer 23b has a larger thickness than the platinum layer 23a. The tungsten layer 23b is deposited by using a CVD method. The platinum layer 23a is deposited by using a sputtering method. See Schindler's col. 4, lines 31-51.

However, Schindler does not teach or suggest that the second film 23b has sufficient oxidation resistance and since the suction of oxygen does not occur, the advantage and use of depositing the second metal film 23b by using a sputtering method and depositing the first metal film 23a by using a CVD method. Schindler therefore does not recognize the features or advantages of the present application. Additionally, Schindler does not teach or suggest a ruthenium film as the upper electrode.

In other words, Schindler does not relate to oxidation formed between a plug 26 and the upper electrode 23 and does not recognize that hydrogen permeates through the first metal film 23a and reaches a dielectric layer 22. As such, Schindler does not recognize the features of the present application as well as the advantages of those features.

Finally, Onishi describes forming an upper electrode of a capacitor having a Pt film 15 as a first metal film, a TiN film 16 as a second metal film and an Al film 17 as a third metal film. The Pt film 15, the TiN film 16 and the Al film 17 are deposited by using a CVD method or a sputtering method. See Onishi's col. 6, line 62- col. 7, line 4.

However, Onishi does not teach or suggest that the third metal film 17 has sufficient oxidation resistance and since the suction of oxygen does not occur, the

advantage and use of depositing the second metal film 16 by using a sputtering method and depositing the first metal layer 23a by using a CVD method. Additionally, Onishi does not teach or suggest a ruthenium film as the upper electrode.

In other words, Onishi also does not relate to oxidation formed between a plug and the upper electrode and does not recognize that hydrogen permeates through the first metal film 15 and reaches a dielectric layer 14. As such, Onishi does not recognize the features of the present application as well as the advantages of those features

Accordingly, the combination of Fan, Schindler and Onishi do not teach or suggest all the features of independent claim 20, and the other independent claims. More specifically, the combination does not teach or suggest, as recited in independent claim 20, depositing a dielectric capacitance insulating film to cover the first electrodes, depositing further a ruthenium film and a conductor layer by a spattering method, patterning the ruthenium film and conductor layers to form second electrodes, and depositing a third inter-layer insulating film covering the second electrodes as recited in independent claim 20. Independent claim 20 therefore defines patentable subject matter. Claim 21 depends from claim 20 and therefore also defines patentable subject matter at least for this reason.

Additionally, the cited references do not teach or suggest, as recited in independent claim 22, forming second electrodes over a capacitance insulating film, forming a second insulating film on the second electrodes, forming an opening for exposing a part of the second electrodes into the second insulating film by using a photoresist film as a mask, ashing the photoresist film and forming a conductor layer inside the opening. Additionally, the cited references do not teach or suggest, as

recited in independent claim 22, forming a ruthenium film by a chemical vapor phase growing method containing oxygen over the capacitance insulating film and forming a metal layer not containing oxygen over the ruthenium film where the ruthenium film directly contacts to the metal layer. Independent claim 22 therefore defines patentable subject matter. Claims 24 and 25 depend from claim 22 and therefore define patentable subject matter at least for this reason.

Independent claim 26 defines patentable subject matter for at least similar reasons as discussed above. Independent claim 26 additionally recites forming the metal layer having a greater film thickness than the ruthenium film over the ruthenium film, and the metal layer has lower resistivity than the ruthenium film where the metal layer has higher oxidation resistance than the ruthenium film. Independent claim 26 therefore defines patentable subject matter. Claim 28 depends from claim 26 and therefore defines patentable subject matter at least for this reason.

Independent claim 29 defines patentable subject matter for at least similar reasons. Claims 30-34 depend from claim 29 and therefore also define patentable subject matter.

For at least the reasons set forth above, each of claims 20-22, 24-26 and 28-34 define patentable subject matter. Withdrawal of the outstanding rejections is respectfully requested.

## CONCLUSION

In view of the foregoing, it is respectfully submitted that the above-identified application is in condition for allowance. Favorable consideration and prompt allowance of the claims are respectfully requested.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (referencing case No. 501.39149X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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**Version with markings to show changes made**

**IN THE CLAIMS:**

Claims 20-22, 24-26 and 28-34 have been amended as follows:

20. (Twice Amended) A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming bit lines and a first layer wiring over MISFET on a main plane of a semiconductor substrate through a first inter-layer insulating film, forming a second inter-layer insulating film and an electrode-forming insulating film, and etching holes in said electrode-forming insulating film;

(b) forming a metal or a metal compound for providing on an inside of said holes, and then forming cylindrical first electrodes by forming a metal film or a metal compound film covering the inner wall of said holes;

(c) depositing a dielectric capacitance insulating film to cover said first electrodes, and depositing further [a first conductor layer] a ruthenium film and a [second] conductor layer by a spattering method;

(d) patterning said [first] ruthenium film and [second] conductor layers to form second electrodes; and

(e) depositing a third inter-layer insulating film covering said second electrodes, and forming a first connection hole reaching said second electrode and a second connection hole reaching said first layer wiring, by etching,

wherein said [second] conductor layer comprises a tungsten film and said third inter-layer insulating film comprises a silicon oxide film.

21. (Twice Amended) A method of producing a semiconductor integrated circuit device according to claim 20, wherein, after said second conductive layer is etched, said [first conductive layer] ruthenium film is etched by using said [second]

conductive layer, that is patterned, as a mask.

22. (Twice Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming first electrodes on a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrode;

(c) forming second electrodes over said capacitance insulating film;

(d) forming a second insulating film [having an opening for exposing a part of said second electrode,] on said second [electrode; and] electrodes;

(e) forming [a first conductor layer inside said] an opening[; wherein:] for exposing a part of said second electrodes into said second insulating film by using photoresist film as a mask;

(f) ashing said photoresist film; and

(g) forming a conductor layer inside said opening;

wherein the formation step of said second electrode includes the steps of:

(i) forming [a first metal layer] a ruthenium film by a chemical vapor phase growing method containing oxygen over said capacitance insulating film; and

(ii) forming a [second] metal layer not containing oxygen over said [first metal layer] ruthenium film,

wherein said [first conductor layer] ruthenium film directly contacts to said [second] metal layer.

24. (Amended) A method of producing a semiconductor integrated circuit device according to claim 22, wherein said [second] metal layer comprises a

tungsten film or a tungsten nitride film.

25. (Amended) A method of producing a semiconductor integrated circuit device according to claim 22, wherein said [second] metal layer is formed by a sputtering method.

26. (Twice Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; [and]

(c) forming continuous second electrodes with respect to a plurality of said first electrodes, over said capacitance insulating film;

(d) forming a second insulating film in order to cover said second electrodes;

(e) forming a hole for exposing a part of said second electrodes into said second insulating film by using photoresist film as a mask;

(f) ashing said photoresist film; and

(g) forming a conductor layer inside said hole;

wherein the formation step of said second electrodes includes the steps of:

(i) forming a [first metal layer] ruthenium film over said capacitance insulating film; and

(ii) forming a [second] metal layer having a greater film thickness than said [first metal layer] ruthenium film over said [first metal layer] ruthenium film, and said [second] metal layer has a lower resistivity than said [first metal layer] ruthenium film,

wherein said metal layer has higher oxidation resistance than said ruthenium film.

28. (Amended) A method of producing a semiconductor integrated circuit device according to claim [27] 26, wherein [said first metal layer is a platinum film or a ruthenium film, and] said [second] metal layer is a tungsten film or a tungsten nitride film.

29. (Twice Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming a continuous second electrode with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrode includes the steps of:

(i) forming a [first metal layer] ruthenium film over said capacitance insulating film in such a fashion as to provide within the spaces between said mutually spaced-apart first electrodes by using a CVD method; and

(ii) forming said [second] metal layer over said first metal layer;

wherein said metal layer has higher oxidation resistance than said ruthenium film.

30. (Amended) A method of producing a semiconductor integrated circuit device according to claim 29, wherein said [second] metal layer is formed by a

sputtering method.

35 ~~31~~. (Amended) A method of producing a semiconductor integrated circuit device according to claim 29, wherein said [second] metal layer comprises a [third] first metal layer formed by a sputtering method and a [fourth] second metal layer formed by a chemical vapor phase growing method over said [third] first metal layer.

32. (Amended) A method of producing a semiconductor integrated circuit device according to claim 29, wherein the film thickness of said [second] metal layer is greater than that of said [first metal layer] ruthenium film.

33. (Amended) A method of producing a semiconductor integrated circuit device according to claim 29, wherein [said first metal layer is a platinum film or a ruthenium film, and] said [second] metal layer is a tungsten film or a tungsten nitride film.

34. (Amended) A method of producing a semiconductor integrated circuit device according to claim 29, wherein said [first metal layer] ruthenium film comprises a [third metal layer] first ruthenium film formed by a sputtering method and a [fourth metal layer] second ruthenium film formed by a chemical vapor phase growing method over said [third metal layer] first ruthenium film.